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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,233	03/27/2001	Ryo Kubota	Q62494	8072

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SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W.
Washington, DC 20037

EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/817,233	KUBOTA ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9 and 12-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9 and 12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Hsien Ming Lee 6/25/2004

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. The objection to claim 1 is withdrawn.

2. Claims 1-7, 9 and 12-22 are pending in the application.

Claim Objections

3. Claim 22 is objected to because of the following informalities: editorial error. At line 4, "on sand upper surface" should be – on said upper surface --. In addition, the term "said second capacitor dielectric film" (last line) lacks antecedent basis.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7, 9 and 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (US 5,858,831) in view of applicants' admitted prior art ("AAPA") and JP H11-284139 (submitted by the applicant).

In re claims 1-3, 5-7 and 16-18, Sung teaches the claimed method of manufacturing a system-on-chip semiconductor device, including a CMOS logic circuit 50 and a DRAM 60 on a same semiconductor chip (col. 1, lines 64-67), comprising:

- providing a CMOS logic circuit portion 50 and a DRAM portion 60 pf a substrate 1;

- forming a first transistor on the substrate 1 at the CMOS logic circuit portion 50 (Fig. 10);
- forming a second transistor on a substrate 1 at the DRAM portion 60 (Fig. 10);
- forming an interlayer film 29 and 34 on the substrate 1 at the CMOS logic circuit portion 50 and on the substrate 1 at the DRAM portions 60, covering the first transistor and the second transistor (Fig. 18);
- forming a groove 36 in the interlayer film 29/34 by removing a portion of the interlayer film 29/34 at the DRAM portion 60 (Fig.18);
- forming a first polysilicon film 37 on an upper surface of the interlayer film 34/29 at the CMOS logic circuit portion 50 and at the DRAM portions 60, and a second polysilicon film 37 on an inner wall of the groove 36 at the DRAM portion 60 (Fig. 18);
- forming a first HSG on a surface of the first polysilicon film and a second HSG on a surface of the second polysilicon film (col. 7, lines 52-54);
- removing the first HSG and the first polysilicon film (Fig.18);
- forming a capacitor dielectric film 38 on the second HSG film (Fig. 18); and
- forming an upper electrode 39 on the capacitor dielectric film 38 (Fig.18).

Sung also teaches that forming the first and the second transistors include forming a first 7 (thickness: 40~60) and a second gate insulating layer 8 (thickness: 50~70) (Fig. 8; col. 4, lines 21-25); the second transistor comprises a peripheral circuit transistor and a switching transistor, wherein both transistor have similar structure; wherein the step of forming the interlayer film 34/29 comprises the steps of forming a first silicon oxide

29 and a second silicon oxide 34 film; the method further comprising the steps of forming an opening in the first interlayer 29 over a diffusion region 31 of the switching transistor (Fig. 15); forming a capacitor electrode 33 in the opening in the first interlayer film 29 (Fig.17), wherein the capacitor electrode 33 is connected to the diffusion region 31 of the switching transistor (Fig. 17); the groove 36 is formed in the second interlayer film 34 (Fig. 17) and the second polysilicon 37 is connected to the capacitor electrode 33 (Fig. 18); forming a capacitor film 38 on the first HSG film (not shown); and forming an upper electrode 39 on the capacitor film 38 (Fig. 19);

Sung also inherently teaches a step of " removing said first HSG and said first polysilicon film" as recited in claim 1. The first HSG and the first polysilicon film 37 is formed on the surface of the interlayer film 34 outside the groove 36 (It is a *processing consequence* of the polysilicon layer 37 deposition and HSG formation, col. 7, lines 47-54.); and the second polysilicon film 37 is formed on the inner wall of the groove 36 at the DRAM portion 60. As illustrated in Fig. 18, said first HSG and said first polysilicon film have been *removed from the surface of the interlayer 34* and only the second polysilicon film 37 and the second HSG are left in the groove 36.

Sung does not teach forming a capacitor dielectric film 38 on the second HSG film **after removing** the first HSG and the first polysilicon film.

However, JP H11-284139, in an analogous art as admitted in the specification page 7, first paragraph, teach forming a groove 40 in interlayer film 44; forming a first polysilicon film 50 on upper surface of the interlayer film 44; forming a first HSG on a surface of the first polysilicon film 50 and a second HSG on a surface of the second polysilicon film within the groove 40 (Fig.4); forming a sacrificial film 54 over the first

HSG on the upper surface of the interlayer film 44 and over the second HSG within the groove 40 (Fig.5); **removing the first HSG and the first polysilicon 50 from the upper surface of the interlayer film 44** (Fig.6); removing the remaining sacrificial film 54; and **then** forming a capacitor dielectric film 56 **after removing** the first HSG and the first polysilicon film 50 (Fig.7); and forming an upper electrode 58 on the capacitor dielectric film 56 (Fig.7).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to modify Sung's method by **first** removing the first HSG and the first polysilicon from the upper surface of the interlayer film **prior to** forming the capacitor dielectric film, as taught by JP-H11-284139, since by this manner it would form a satisfactory crown-type capacitor.

In re claim 22, Sung in view of JP-H11-284139 also teach forming said capacitor dielectric film comprises a step of forming a first capacitor dielectric film 38 on said upper surface of said interlayer film 34/29 and a second capacitor dielectric film 38 on said second HSG within the groove 36 after removing said first HSG and said first polysilicon film from the upper surface of the interlayer film (as suggested by JP-H11-284139); and forming an upper electrode comprising forming an upper electrode 39 on said capacitor dielectric film 38.

In re claims 4, 12, 13 and 19, Sung does not teach forming a BPSG over the first interlayer film 29 as the second interlayer film 34.

AAPA, however, teaches utilizing the BPSG as the second interlayer film 120 over the first interlayer film 116 (SiO2; Figs. 3C-3D) in the DRAM portion.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to replace the silicon oxide of Sung with the BPSG of AAPA used as the second interlayer, since by doing so it would provide a better planarization for the subsequent processing steps.

In re claim 9, Sung does not expressly teach the capacitor dielectric film 38 comprising Ta2O5 but does suggest that the capacitor dielectric film 38 can be an insulator with a high dielectric constant (col. 7, lines 55-57).

AAPA, however, teaches utilizing a high-dielectric-constant material such as Ta2O5 for capacitor dielectric film in DRAM application (page 2, lines 12-13).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize the high-dielectric-constant material such as Ta2O5, as suggested by AAPA, for capacitor dielectric film in the method of Sung, since by doing so it would improve the performance of the capacitor.

In re claims 14 and 15, the selection of the surface area ratio of the memory cell portion is obvious because it is a matter of determining optimum process condition by routine experimentation for best results for the DRAM performance in conjunction with the consideration the size of CMOS logic circuit portion. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In fact, AAPA teaches that the ration of memory cells 1 to the area of the chip 2 can be 50~60% (Fig. 6A; page 12, lines 14-16). In such situation, the applicants must show that the particular range is critical,

generally by showing that the claimed range achieves unexpected results relative to the prior art range. See M.P.E.P. 2144.05 III

In re claims 20-21, Sung in view of AAPA teaches that the first transistor comprises an n-type transistor having a gate electrode which is made of doped polysilicon and the second transistor comprises a p-type transistor having a gate electrode which is made of doped polysilicon.

Response to Arguments

6. Applicant's arguments filed 4/21/04 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of JP H11-284139, as stated above.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Primary Examiner
Art Unit 2823

June 25, 2004

Hsien Ming Lee
6/25/2004